TGA2586-FL

7.9–8.4 GHz 50 W GaN Power Amplifier

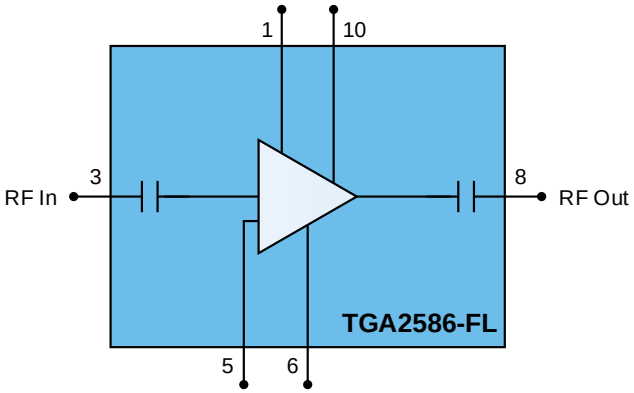
General Description

Qorvo's TGA2586-FL is a high power GaN amplifier operating between 7.9 and 8.4 GHz. it can deliver greater than 47 dBm of saturated output power with 36% power-added efficiency and 14 dB small signal gain.

Ideally suited for satellite communications, the TGA2586-FL is packaged in a carrier plate, flanged package for superior thermal management.

The TGA2586-FL uses Qorvo's proven TQGaN25 process which provides superior performance while maintaining high reliability. In addition, the use of SiC substrates provides optimum thermal performance necessary for reliable high power operation.

Functional Block Diagram



Product Features

- Frequency Range: 7.9–8.4 GHz
- P_{SAT}: 47 dBm (CW)
- P_{1dB}: 43 dBm
- PAE: 36%
- Small Signal Gain: 14 dB
- Bias: V_D = 24 V, I_{DQ} = 2.24 A, V_G = -2.4 V Typical
- Integrated Thermistor Temperature Monitor
- Package Dimensions: 17.4 x 24.0 x 3.9 mm

Pad Configuration

Pad no.	Symbol
1	V_G
2, 4, 7, 9	N/C
3	RF_{IN}
5	Temp (Thermistor)
6	V_D
8	RF_{OUT}
10	V_D

Applications

- Satellite Communications

Ordering Information

Part	Description
TGA2586-FL	GaN High Power Amplifier, Waffle Pack, Qty 10

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Drain to Gate Voltage (V_D-V_G)	100 V
Gate Voltage Range (V_G)	-5 to 0 V
Drain Current (I_D)	10 A
Gate Current (I_G)	-23 to 56 mA
Power Dissipation (P_{DISS})	100 W
RF Input Power, CW, 50 Ω, T = 25 °C (P_{IN})	+44 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value/Range
Drain Voltage (V_D)	24 V
Drain Current (I_{DQ})	2240 mA
Drain Current Under RF Drive (I_{D_Drive})	5800 mA
Gate Voltage (V_G)	-2.4 V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

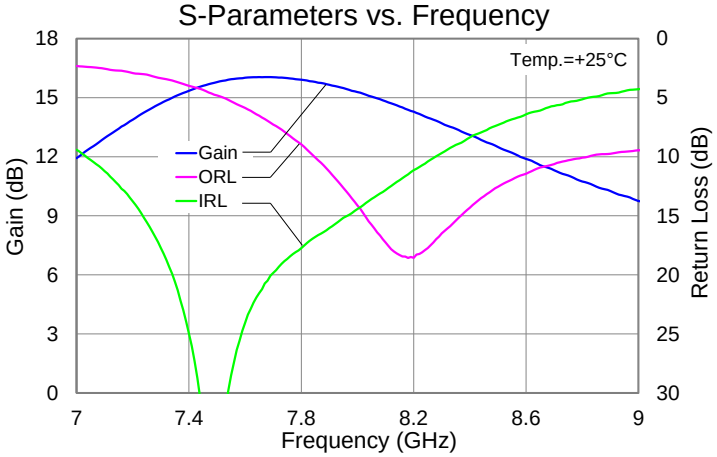
Test conditions unless otherwise noted: 25 °C, V_D = 24 V, I_{DQ} = 2240 mA , V_G = -2.4 V Typical. Data de-embedded to reference lines.

Parameter	Min	Typical	Max	Units
Operational Frequency Range	7.9		8.4	GHz
Small Signal Gain		14		dB
Input Return Loss		9		dB
Output Return Loss		15		dB
Output Power at Saturation (P_{IN} = 37 dBm)		47		dBm
Power-Added Efficiency (P_{IN} = 37 dBm)		36		%
Output TOI		48		dBm
Gain Temperature Coefficient		-0.016		dB/°C
Power Temperature Coefficient		-0.006		dBm/°C
TOI Temperature Coefficient		-0.008		dBm/°C

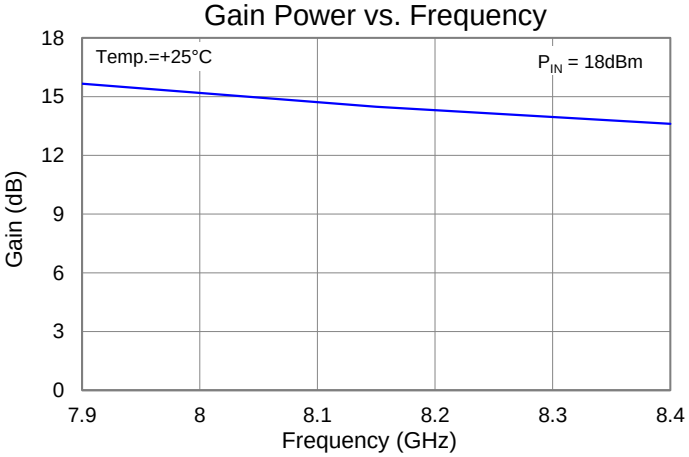
Typical Performance

Conditions unless otherwise specified: V_D = 24 V, I_{DQ} = 2.24 A, V_G = -2.4 V Typical, CW

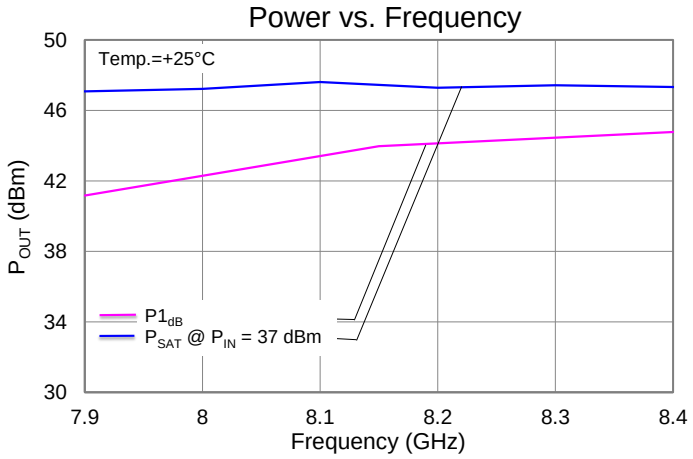
S-Parameters vs. Frequency



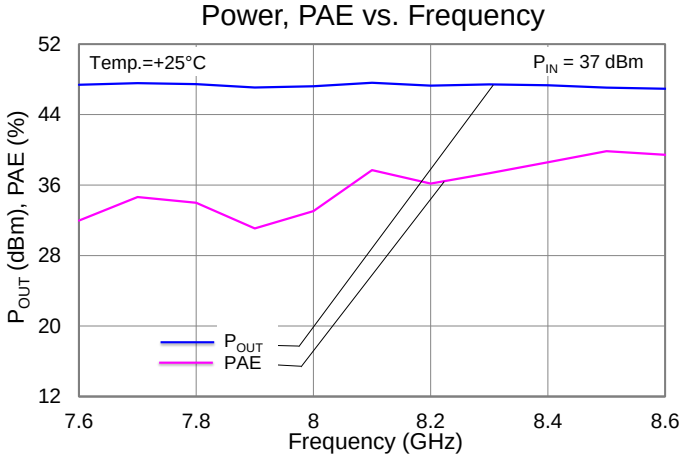
Gain Power vs. Frequency



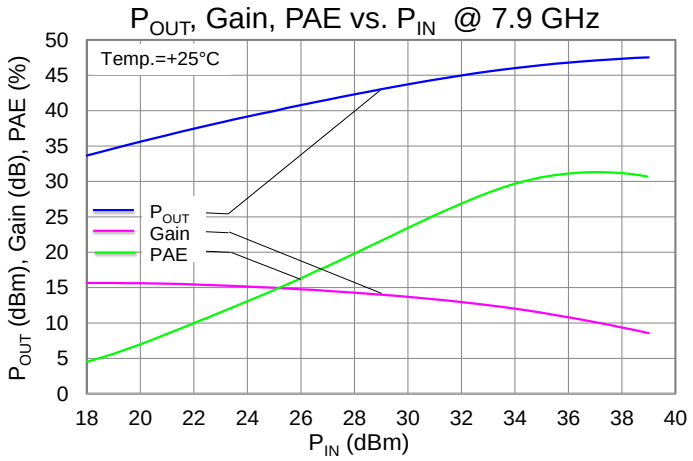
Power vs. Frequency



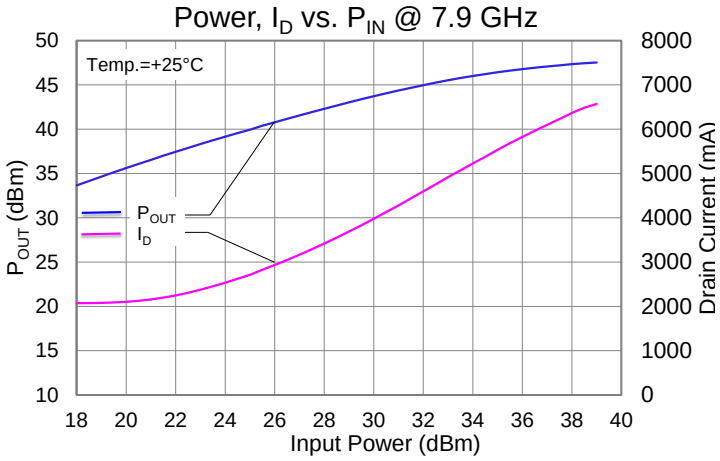
Power, PAE vs. Frequency



P_{OUT}, Gain, PAE vs. P_{IN} @ 7.9 GHz

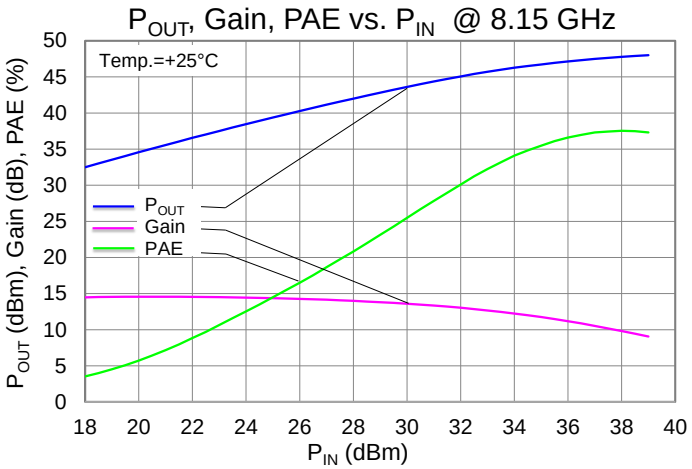


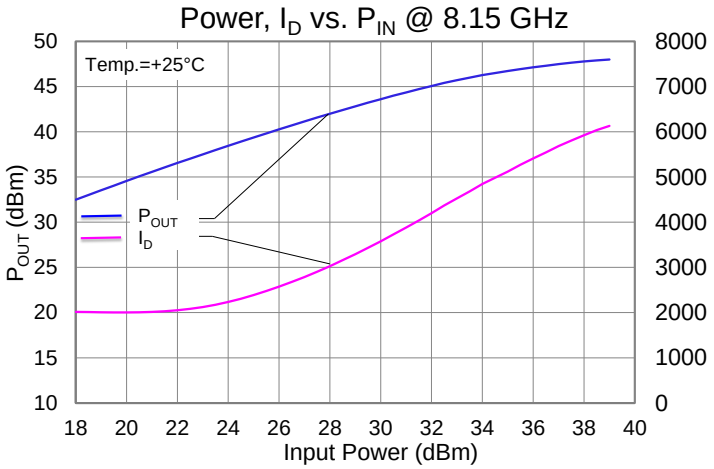
Power, I_D vs. P_{IN} @ 7.9 GHz

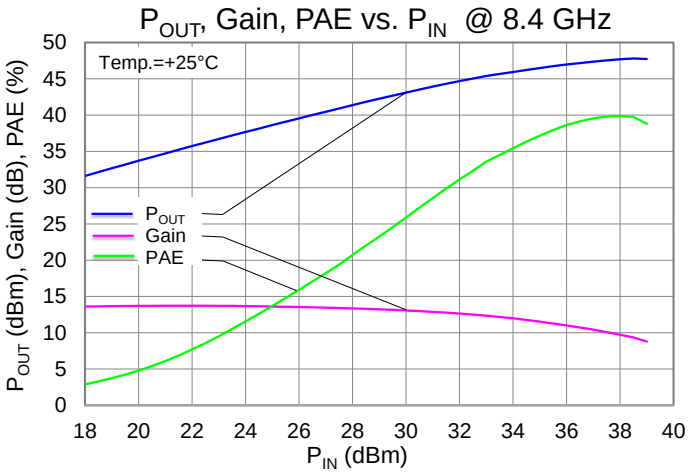


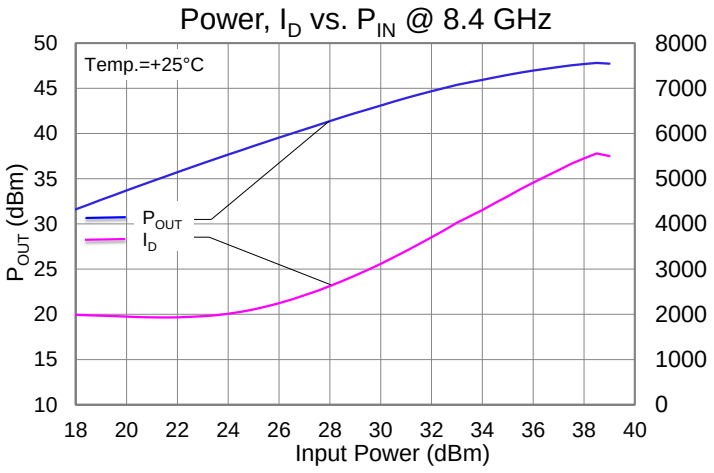
Typical Performance

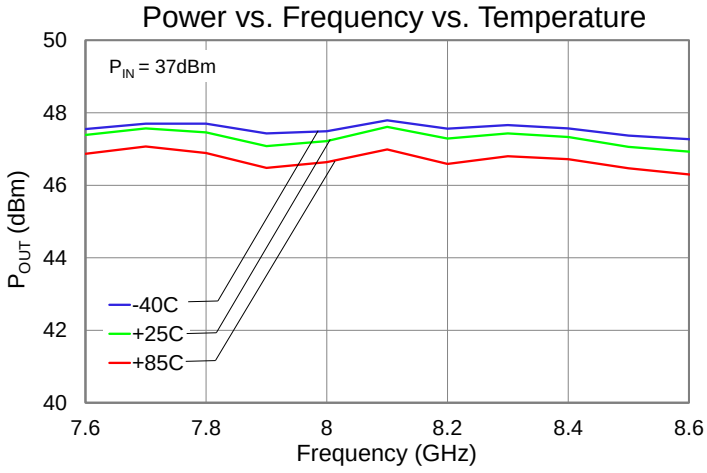
Conditions unless otherwise specified: V_D = 24 V, I_{DQ} = 2.24 A, V_G = -2.4 V Typical, CW

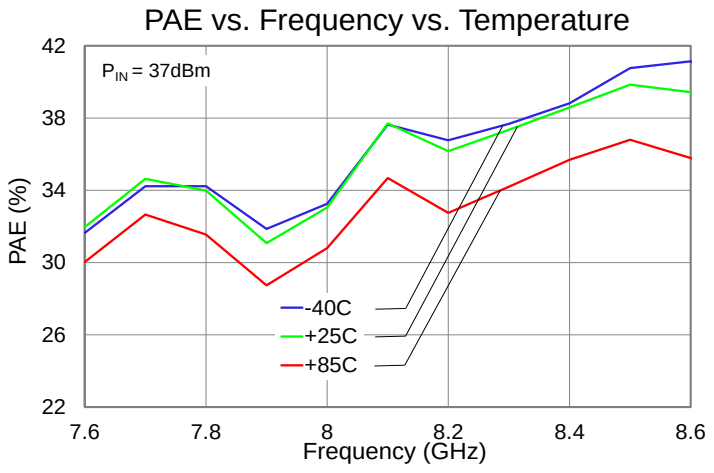








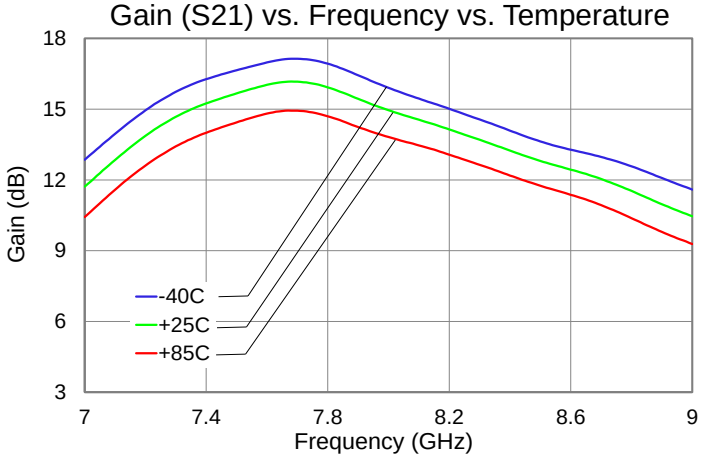




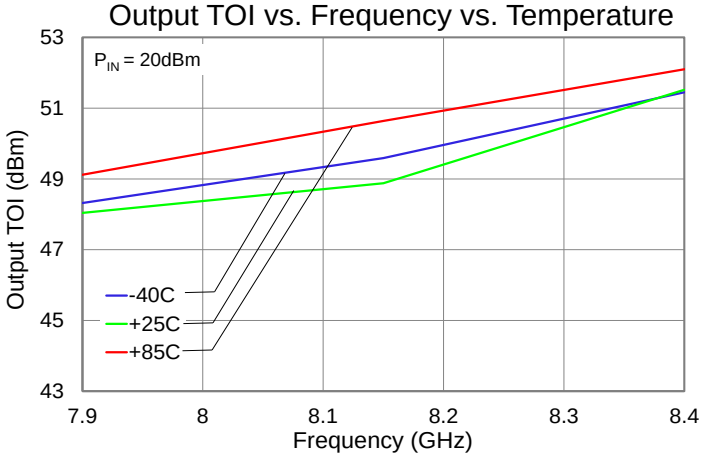
Typical Performance

Conditions unless otherwise specified: V_D = 24 V, I_{DQ} = 2.24 A, V_G = -2.4 V Typical, CW

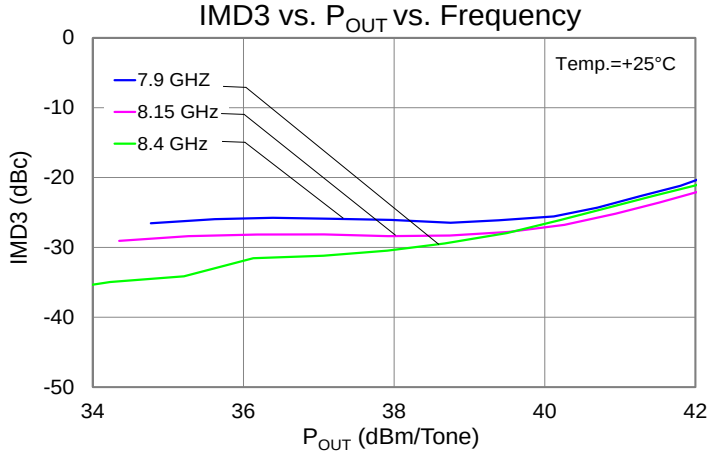
Gain (S21) vs. Frequency vs. Temperature



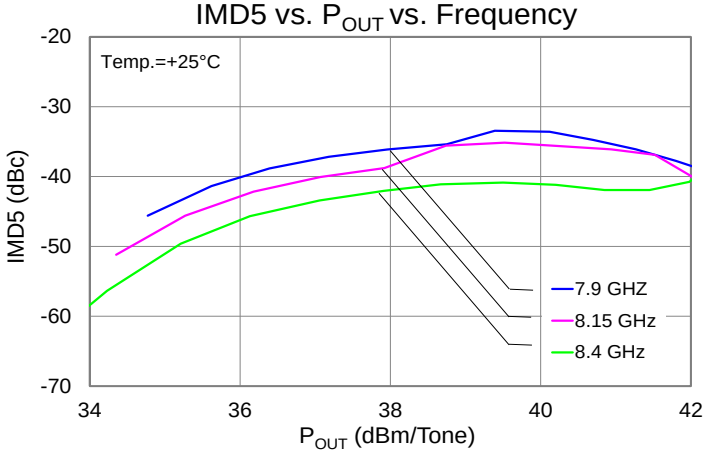
Output TOI vs. Frequency vs. Temperature



IMD3 vs. P_{OUT} vs. Frequency



IMD5 vs. P_{OUT} vs. Frequency



Typical Performance

A 100K Ω thermistor is assembled inside the TGA2586-FL package. Nominal resistance versus temperature is shown in the table below. This resistance measurement is taken between the Temp pin and ground pin to provide a useful indicator of the maximum package temperature.

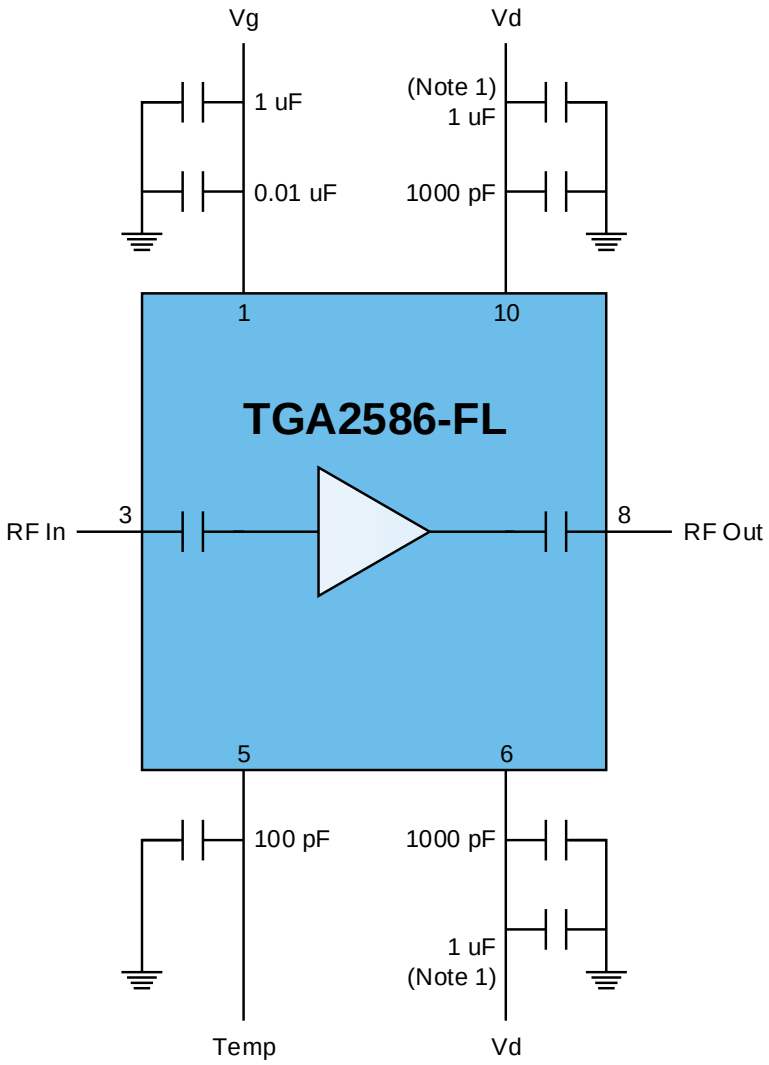
deg C	R (Kohm)	deg C	R (Kohm)
0	378.80	65	17.89
5	284.71	70	14.84
10	216.16	75	12.37
15	165.70	80	10.37
20	128.17	85	8.74
25	100.00	90	7.40
30	78.66	95	6.29
35	62.36	100	5.37
40	49.81	105	4.61
45	40.06	110	3.96
50	32.44	115	3.43
55	26.44	120	2.97
60	21.68	125	2.59

Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	Tbaseplate = 85 °C, V_D = 24 V, I_{DQ} = 2240 mA P_{DISS} = 54 W	1.27	°C/W
Channel Temperature (T_{CH}) (Without RF Drive)		153.6	°C
Thermal Resistance (θ_{JC}) (1)	Tbaseplate = 85 °C, V_D = 24 V, I_{D_Drive} = 5800 mA P_{OUT} = 47.6 dBm, P_{DISS} = 82 W CW Operation.	1.21	°C/W
Channel Temperature (T_{CH}) (Under RF Drive)		184.2	°C

Notes:
1. Thermal resistance measured to back of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Application Circuit



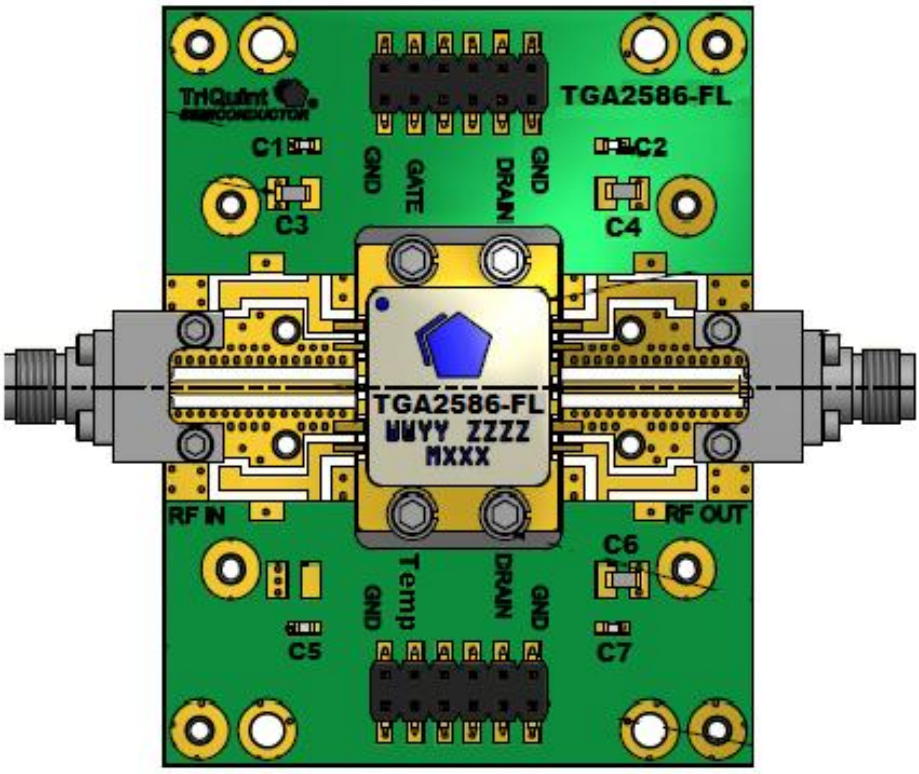
Notes:

1. The drain by-pass caps can be removed for drain pulsing. Drain voltage must be biased from both sides top and bottom V_D pins.
2. To prevent damage to the device due to bias overshoot or oscillation, we recommend setting current limits for all power supplies before applying the voltage as listed below.

Bias-up Procedure	Bias-down Procedure
Apply -5.0 V to V_G, set 10 mA current limit to V_G.	Turn off RF signal
Apply +24 V to V_D, set 8 A current limit to V_D.	Reduce V_G to -5.0 V. Ensure I_{DQ} ~ 0 mA
Adjust V_G until I_{DQ} = 2240 mA (V_G ~ -2.4 V Typ.)	Set V_D to 0 V
Turn on RF supply	Set V_G to 0 V

Recommended Board Layout Assembly

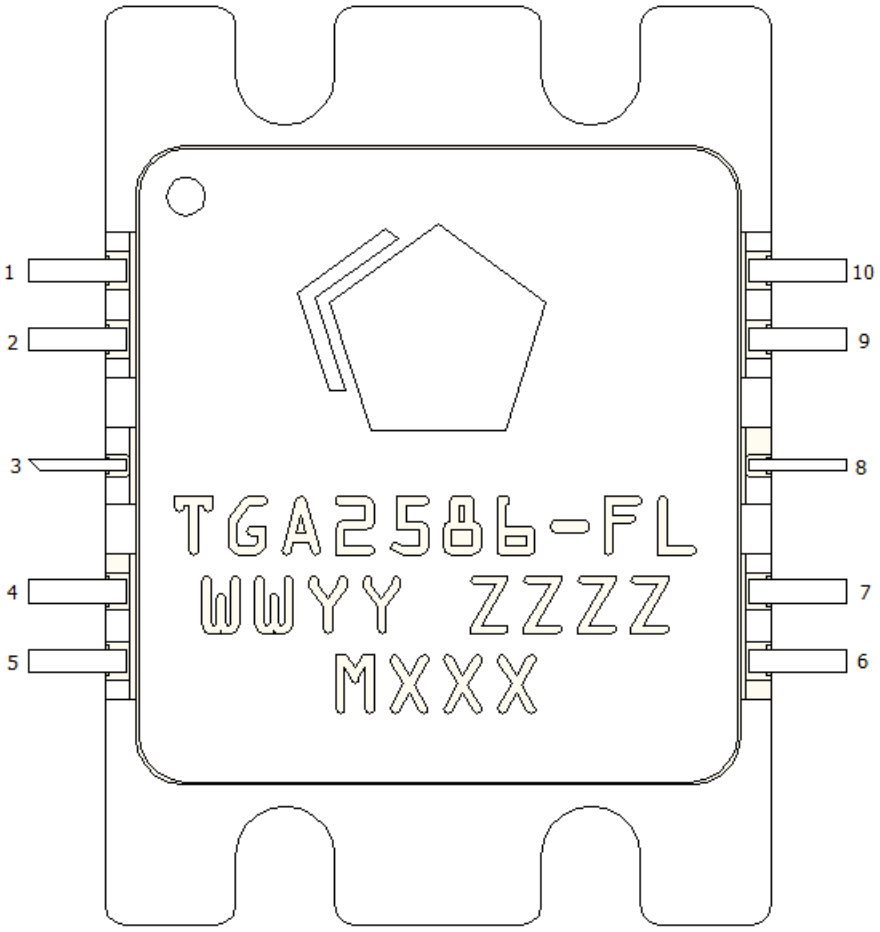
Top dielectric material is RO4350 0.020 inch thickness with 0.5 oz. copper.



Bill of Materials

Reference Design	Value	Description	Manufacturer
C1	0.01 uF	Cap, 0603, 50 V, 10%	Various
C2, C7	1000 pF	Cap, 0603, 50 V, 5%	Various
C3	1.0 uF	Cap, 1206, 16 V, 10%	Various
C4, C6	1.0 uF	Cap, 1206, 50 V, 10%, XR7	Various
C5	100 pF	Cap, 0603, 50 V, 5%	Various

Pin Layout

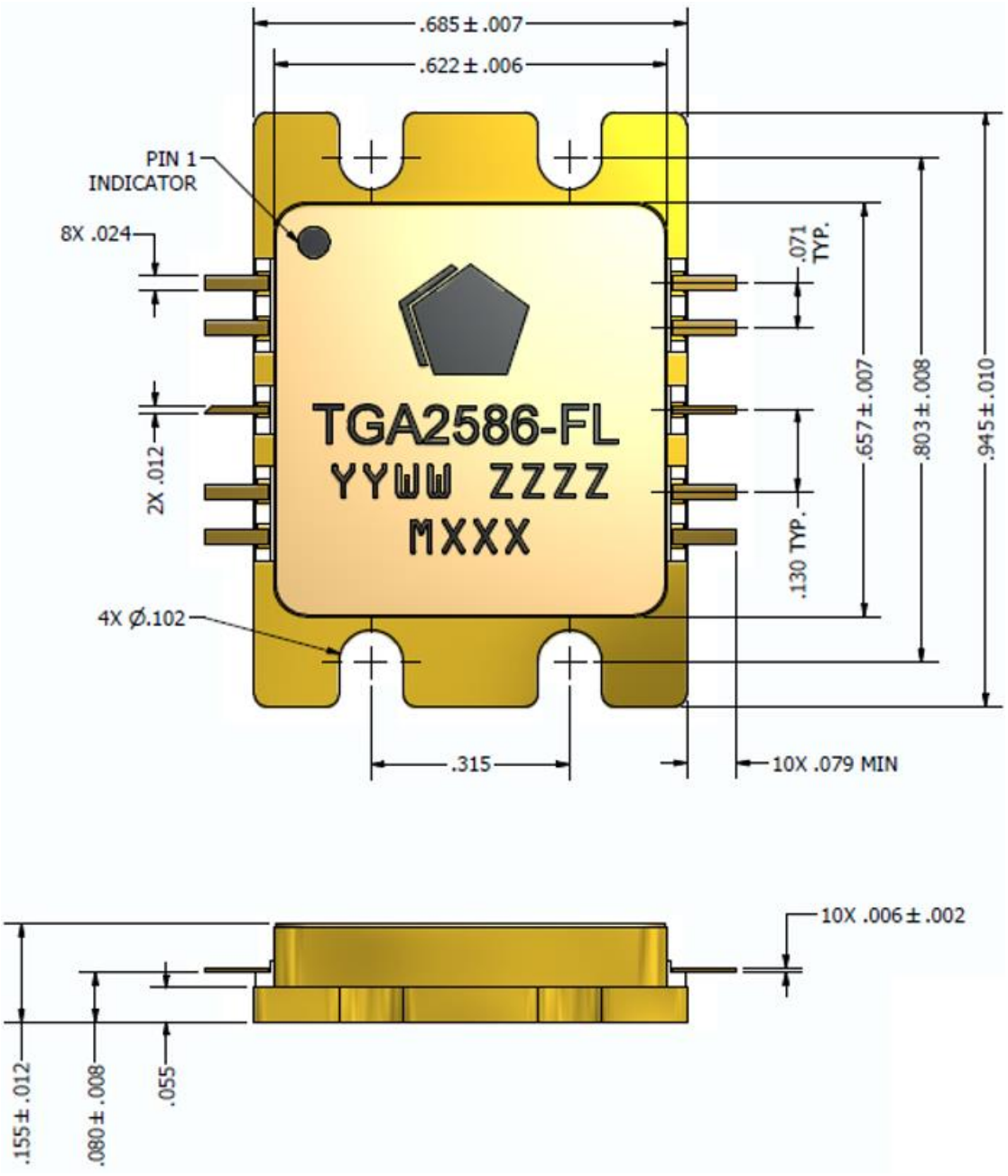


Pin Description

Pin	Symbol	Description
1	V_G	Gate voltage. Bias network is required(1)
2, 4, 7, 9	N/C	No internal connection; must be grounded on PCB.
3	RF_{IN}	RF input, DC blocked.
5	TEMP	Temperature sensing pin (Thermistor)(2)
6	V_D	Bottom Drain voltage. Bias network is required(1)
8	RF_{OUT}	RF output, DC blocked.
10	V_D	Top Drain voltage Bias network is required(1)

Notes:
1. See Application Circuit on page 8 as an example.
2. See page 6 for addition thermal information.

Mechanical Information



1. All dimensions are in inches, unless specified otherwise.
2. Marking: Part number–TGA2586-FL, Week/Year code–WWYY, Serial Number-ZZZZ, Batch ID–MXXX.
3. All metalized features are gold plated.
4. Package is an all metal design with ceramic feed thru's.
5. Part is hermetically sealed.

Solderability

Compatible with the latest version of J-STD-020, lead free solder, 260 °C

Assembly Notes

1. Clean the board or module with alcohol. Allow it to fully dry.
2. Nylock screws are recommended for mounting the TGA2586-FL to the board.
3. To improve the thermal and RF performance, we recommend the following:
   a. Apply thermal compound or 4 mils indium shim between the package and the board.
   b. Attach a heat sink to the bottom of the board and apply thermal compound or 4 mils indium shim between the heat sink and the board.
4. Apply solder to each pin of the TGA2586-FL.
5. Clean the assembly with alcohol.

Handling Precautions

Parameter	Rating	Standard
ESD-Human Body Model (HBM)	2	JEDEC/JESD22-A114

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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